REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-31 are pending in this application. No claim amendments are presented, thus no new matter is added.

In the outstanding Office Action, the specification was objected to because of a minor informality; Claims 1 and 23-27 were rejected under 35 U.S.C. §102(b) as anticipated by Page ("MAC-DSD Multi-channel Audio Connection for DSD"); and Claims 2-22 and 28-31 were objected to as dependent upon a rejected base claim but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Applicant appreciatively acknowledges the indication of allowable subject matter. However, since Applicant considers that independent Claims 1 and 23-27 patentably define over the applied references, the remaining dependent claims are presently maintained in dependent form.

Regarding the objection to the Title, the Title is amended to be more descriptive of the claimed invention. Accordingly, Applicant requests that the objection to the Title be withdrawn.

Claims 1 and 23-27 were rejected under 35 U.S.C. §102(b) as anticipated by Page. Applicant traverses this rejection as independent Claims 1 and 23-27 recite novel features clearly not taught or rendered obvious by Page.

Independent Claim 1 recites a data communications system for communicating a data signal formed of successive data elements. The system includes a transmission node, a reception node, and a link providing a data connection from the transmission node to the reception node. The reception node includes "a clocking-signal transmitter for transmitting a

synchronization clocking signal to said reception node via said link, ***said synchronization clocking signal having synchronizing features occurring at a fre uency lower than a data element rate***" and "an assembler for assembling elements of said data signal into data frames, each data frame having a plurality of successive data elements of said data signal, for transmission to said reception node via said link, ***said assembler being responsive to said synchronization clocking signal so as to set a synchronization flag associated with a data element having a first predetermined temporal relationship with a synchronizing feature of said synchronization clocking signal***." Independent Claim 1 also recites that the reception node includes "a detector for detecting a synchronizing feature of said synchronization clocking signal received from said transmission node… a disassembler for disassembling received data frames to regenerate said data signal, ***said disassembler being operable to detect a data element associated with a set synchronization flag***," and "an output unit for ***outputting a data element associated with a set synchronization flag at a second predetermined temporal relationship with respect to said synchronizing feature of said received synchronization clocking signal***, said first and second predetermined temporal relationships arranged so that a predetermined system latency exists between input of a data element to said transmission node and subsequent output of that data element by said reception node."

Independent Claims 23-27, while directed to alternative embodiments, recite substantially similar features directed to the transmission and/or reception node. Accordingly, the remarks and arguments presented below are applicable to each of independent Claims 1 and 23-27.

Turning to the applied reference, Page describes a configuration of a multi-channel audio connection for DSD (MAC-DSD) that provides a bi-directional, point-to-point

connection for 24 channels of $64f_s$ digital audio. The link uses a single category 5 UTP cable, and is designed for operation in a studio environment.

In rejecting the pending independent claims, the outstanding Office Action relies on an embodiment described in Page in which the Ethernet physical layer is clocked at $576f_s$, which is very near to the normal physical layer clocking rate of 25MHz but is less likely to cause interference with a $64f_s$ audio data clock generator.

More specifically, the outstanding Office Action maps the features of Page to independent Claim 1, as follows:

Data Element Rate	$576f_s$
Synchronization clocking signal	$64f_s$
Synchronizing features occurring at a frequency lower than a data element rate	$64f_s$ clock pulses (see OA p. 3 l. 7) or Frame flags, page 18 (see p. 3 l. 14)
Data Frames	Frame types, p. 14
Assembler	Physical layer interface, PHY
(Reception node) detector	Comparator, Fig. 3
Disassembler	Physical layer interface, PHY
Output unit	MAC-DSD

Applicant, however, respectfully submits that Page fails to teach or suggest various claimed features for which it is asserted.

More specifically, $576f_s$ (25.4 MHz) is not a data element rate. As described at p. 3, for example, the system described in Page carries 24 DSD audio channels, each at $64f_s$, making the payload data rate 67.7Mbit/s. Thus, $576f_s$ is merely a clock speed for a particular device in the link, and $64f_s$ is the data rate of one channel but the link carries 24 such channels.

Further, if the assembler is the physical layer interface, as asserted in the outstanding Office Action, then that unit is not "responsive ... so as to set a synchronization flag associated with a data element having a first predetermined temporal relationship with a synchronizing feature..." as recited in independent Claim 1. The physical layer interface does not have any inputs and outputs apart from the raw data stream. More specifically, all that

the physical layer interface does is format a data stream into Ethernet frames for transmission along a cable, in accordance with the physical layer of the seven-layer OSI model of data links.

The Office Action further asserts that the comparator (Fig. 3) "detects a synchronizing feature ... of the synchronizing clocking signal". However, as described in the text above Fig. 3 on p. 4 of Page, the comparator merely thresholds the received clocking signal to turn it into a logic signal, and does not detect anything. More particularly, if the Office Action interprets the "Frame Flags" as synchronizing features, the comparator is completely blind to these, and moreover, the flags described in Page do not even pass along the twisted pair of wires forming the input to the comparator.

In rejecting the claimed features directed to the dissassembler, Office Action again relies on the receiver's physical layer interface. While this component may convert Ethernet frames into a received data stream, it does not "detect a data element associated with a set synchronization flag". Ethernet physical layer interfaces operate at the physical layer, and simply are not concerned with features of the data being transmitted.

With regard to the claimed "output unit", there is no teaching in Page that the MAC-DSD device of Fig. 3 applies a predetermined temporal relationship between data element output and a received synchronization clocking signal, in such a way that the overall system latency is defined. In contrast, as described at Fig. 15 and in the text immediately below it on p. 17, Page states that "[u]nder normal conditions a data block is output as soon as frame reception has commenced, incurring near-zero receiver latency".

The purpose of the Frame Flags (p. 14 of Page, which the Office Action equates to "synchronization flags" in Claim 1) is to allow the receivers to synchronize their data output with a locally generated f_s clock signal (f_s (B)), as described at Fig. 16 and p. 18. The frame flags do not act as "synchronization flags" as recited in Claim 1, whereby they are compared

to a feature of the received (i.e. generated at the transmitter, not locally generated) clock signal to determine when the samples should be output.

In summary, in Page, frame flags are transmitted to indicate synchronization to the transmitter's f_s clock signal. The data samples are then output with the same synchronization but relative to another f_s clock signal locally generated at the receiver and of arbitrary phase relative to the transmitter's f_s clock signal. The overall system latency is unknown. In contrast, in the present invention: (a) low frequency synchronizing features are transmitted with the data element clock signal, (b) data samples are output at the receiver at a certain time relative to the received synchronizing features, the result being (c) to give a predetermined overall latency to the whole system.

Therefore, for at least the reasons discussed above Page fails to teach or suggest various features recited in pending independent Claims 1 and 23-27. Accordingly, Applicant respectfully requests that the rejection of Claims 1 and 23-27 under 35 U.S.C. §102 be withdrawn.

Consequently, in view of the present amendment and in light of the foregoing comments, it is respectfully submitted that the invention defined by Claims 1-31 patentably define over the applied references. The present application is therefore believed to be in condition for formal allowance and an early and favorable reconsideration of the application is therefore requested.

Respectfully submitted,

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